What is Claimed is:

1. An ESD(Electro-Static Discharge) protection circuit comprising:

a pad and a main chip; and,

a plurality of transistors each connected between the pad and the main chip and having a resistor connected only to an input terminal.

2. An ESD protection circuit comprising:

a substrate;

a transistor formed on the substrate;

a first insulating film formed on the substrate inclusive of the transistor and having a first contact hole to an input terminal of transistor;

a buffered layer formed on the first insulating film inclusive of the first contact hole and electrically connected to the input terminal for acting as a resistor;

a second insulating film formed on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

a pad formed on the second insulating film inclusive of the second contact hole and electrically connected to the buffered layer.

2. A method for fabricating an ESD protection circuit, comprising the steps of:

(1) forming a transistor on a substrate;

(2) forming a first insulating film on the substrate inclusive of the transistor and having a first contact hole to an input terminal of the transistor;

(3) forming a buffered layer in the first contact hole and the first insulating film in the

vicinity of the first contact hole;

(4) forming a second insulating film on the first insulating film inclusive of the buffered layer and having a second contact hole to the buffered layer; and,

(5) forming a pad both on the second contact hole and the second insulating film in the vicinity of the second contact hole.

4. A method as claimed in claim 3, wherein the buffered layer is formed of polysilicon.

5. A method as claimed in claim 3, wherein the buffered layer is formed of a silicide.

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